IN THE CLAIMS:

Presented below are the pending claims.

1. (Previously presented) A transistor device, comprising:

a substrate having a source region, a drain region and a channel region, in which at least one of the source, drain and channel regions has a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region formed over the channel region.

- 2. (Previously presented) The transistor of claim 1 wherein the void is located substantially in a center of the channel region.
- 3. (Previously presented) The transistor of claim 1 wherein the void is approximately 50 nm across.
- 4. (Previously presented) The transistor of claim 1 wherein the void is located at a depth of approximately 1000 angstroms in the channel region.
- 5. (Canceled)
- 6. (Previously presented) The transistor of claim 1 wherein the void is located in the channel region and near an edge of the channel region adjacent to the source region.
- 7. (Previously presented) The transistor of claim 1 wherein the void is located in the channel region near an edge of the channel region adjacent to the drain region.

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- 8. (Previously presented) A transistor, comprising:
 a substrate having a source region, a drain region and a channel region, in
 which a void is located below the source region to place one of the regions into a
 compressive or tensile stress to alter carrier mobility due to the stress; and
 a gate region above the channel region.
- 9. (Previously presented) The transistor of claim 8 wherein a void is also located below the drain region.
- 10. (Previously presented) The transistor of claim 9 wherein the source and drain regions are under compressive stress.
- 11. (Previously presented) The transistor of claim 8 wherein the source region is under tensile stress.
- 12. (Previously presented) The transistor of claim 8 wherein the drain region is under compressive stress.
- 13. (Previously presented) The transistor of claim 8 wherein the gate region is polysilicon.
- 14. (Previously presented) The transistor of claim 8 wherein the gate region is metal.
- 15. (Previously presented) A transistor comprising:
 a substrate having a source region, a drain region and a channel region; and
 a gate region having a void to place the substrate under mechanical stress to
 alter carrier mobility due to the stress.
- 16. (Canceled)

Serial No.: 10/045,376 Filed: 11/9/2001 17. (Previously presented) The transistor of claim 15 wherein the gate region is polysilicon.

18. (Previously presented) The transistor of claim 15 wherein the gate region is metal.

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